

216692US-2



IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

TAKASHI YAMADA ET AL : GROUP ART UNIT: 2826

SERIAL NO. 09/995,594 :

FILED: NOVEMBER 29, 2001 : EXAMINER: DICKEY

FOR: SEMICONDUCTOR CHIP HAVING
MULTIPLE FUNCTIONAL BOCKS
INTEGRATED IN A SINGLE CHIP
AND METHOD FOR FABRICATING
THE SAME

ELECTION

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the Restriction Requirement dated December 24, 2002 Applicant elects Group II, Claims 1-15, drawn to a device, classified in class 257, subclass 347.

Accordingly, examination on the merits of Claims 1-15 is believed to be in order, and an early and favorable action is respectfully requested.

Respectfully submitted,

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MAIER & NEUSTADT, P.C.

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Docket No.: 216692US2

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

RE: Application Serial No.: 09/995,594

Applicants: Takashi YAMADA, et al.

Filing Date: November 29, 2001

For: SEMICONDUCTOR CHIP HAVING MULTIPLE
FUNCTIONAL BLOCKS INTEGRATED IN A
SINGLE CHIP AND METHOD FOR FABRICATING
THE SAME

Group Art Unit: 2826

Examiner: Thomas Dickey

SIR:

Attached hereto for filing are the following papers:

ELECTION

Our check in the amount of **\$0.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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